REMARKS

The Office Action dated May 8, 2003 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claims 1 and 2 are amended. No new matter is added. In view of the following remarks, Applicants request the favorable consideration of claims 1-15.

The Office Action rejected claim 1-15 under 35 U.S.C. §102(b) as being anticipated by Bertin et al. (U.S. Patent No. 5,946,545). The Office Action takes the position that Bertin teaches or suggests all the features recited in claims 1-15. Applicants respectfully disagree.

Claim 1 is directed to a semiconductor memory device comprising a data buffer, a plurality of DRAM cell array blocks, an SRAM redundancy cell, a fuse circuit, a comparison circuit and an I/O bus. The data buffer inputs and outputs data from and to an exterior of the device. The SRAM redundancy cell is disposed at a peripheral portion of a corresponding one of the plurality of DRAM cell array blocks. The fuse circuit stores an address of a defect memory cell in the DRAM cell array blocks. The comparison circuit compares an input address with the address stored in the fuse circuit. The I/O bus couples the SRAM redundancy cell to the data buffer in response to an address match signal from the comparison circuit.

Bertin is directed to high density electronic circuit packaging. Bertin discloses a programmable spare circuit which is built in a multi-chip package. Specifically, Bertin discloses, as illustrated in Figure 6, a stack 113 which includes a plurality of memory chips. Logic circuit 116 including an SRAM serves as a spare for the memory chips. Logic circuit 116 receives address and control inputs 117 from a memory controller or other external processing unit. For instance, logic circuit 116 is shown in Fig. 7 as sparing circuit 180. circuit 180 receives address signals and compared. The fuse networks 196 and 198 store the defective addresses. If an input address does not correspond to the previously encoded failed memory cell location, then a redundant word generator and a redundant bit generator are activated to access the spare memory cell. In other words, if the input address matches one of the defective addresses, access is made to the SRAM 210.

However, Bertin does not teach or suggest an SRAM redundancy cell disposed at a

peripheral portion of a corresponding one of the plurality of DRAM cell array block. Bertin does not teach or suggest an SRAM redundancy cell that is situated inside the same chip that includes the DRAM cells. Accordingly, the claimed invention does not require an address selection circuit and a data-access circuit dedicated to the SRAM, as disclosed in Bertin. As a result, the claimed invention provides the benefit of avoiding unnecessary power consumption and the efficient use of space. The features recited in claim 1 nor the benefits associated from the claimed invention are neither taught nor suggested by the applied reference. Thus, Bertin neither teaches nor suggests a SRAM redundancy cell disposed at a peripheral portion of a corresponding one of the plurality of DRAM cell array blocks. In view of these distinctions, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 102(b).

Claims 2-15 depend upon independent claim 1. In regard to claims 2-8, the Office Action takes the position that the positioning of SRAM redundancy cell is disclosed in Bertin. However, Bertin discloses merely the construction of a multi-chip package. Bertin does not teach or suggest the positioning features inside a semiconductor memory device. Thus, Bertin does not teach or suggest the specific locations of the SRAM redundancy cell inside the semiconductor memory device as recited in claims 2-8. Additionally, since claims 2-15 depend upon independent claim 1, it is submitted that these claims, for at least the reasons mentioned above, likewise recite subject matter that is neither taught nor suggested by the applied references. Therefore, Applicants request the withdrawal of the rejection of claims 2-15 under 35 U.S.C. 102(b).

In view of the amendments to the claims and the distinctions discussed above, withdrawal of the rejections to claims 1-15 is respectfully requested. Claims 1 and 2 are amended. No new matter is presented. Therefore, Applicants submit that the application is now in condition for allowance with claims 1-15 contained therein.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

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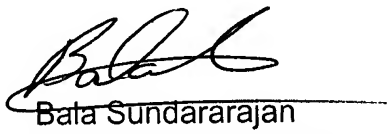

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Enclosure: